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| EXAMINER | |
|---|---|
| QUILLEN, ALLEN E | |

| ART UNIT | PAPER NUMBER |
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| 2676 | 4 |

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/966,970 | Applicant(s) HARPER, JEFFREY D. | |
|---|---|---|---|
| | Examiner Allen E. Quillen | Art Unit 2676 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's arguments with respect to claims 1, 7, 15 have been considered but are moot in view of the new ground(s) of rejection. Claim 1 is amended. No claims are cancelled, all 27 of them are still pending. The Applicant's well organized response is especially noted.

### *Drawings*

2. New drawings are received.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roth, et al, U.S. Patent 5,818,528, Shand, U.S. Patent 5,692,159, in view of Anderson et al, U.S. Patent 6,567,122.

5. Regarding claim 1, Roth discloses an imaging device for simultaneous capture and image display (Figure 1, Column 7, lines 24-27; Column 16, lines 48-66; Figure 22, Column 25, lines 2-12), the device comprising: an imager (Column 3, lines 45-67) for capturing image data upon aiming the imager at an image (Column 7, lines 22-38); a central processing unit (CPU) that is in communication with the imager and issues commands to capture image data (Figure 8, Column 14, lines 45-60).

Roth discloses two memories (Column 4, lines 40-55) but does not disclose a direct memory access module in communication with the imager and the CPU that executes the commands to capture image data; and a memory module in communication with the CPU and the DMA module, the memory module including a first image capture buffer that temporarily stores first-in-time captured image data prior to displaying first-in-time image data and a second image capture buffer that temporarily stores second-in-time captured image data prior to displaying second-in-time image data. Shand teaches a direct memory access module in communication with the imager and the CPU that executes the commands to capture image data (Column 4, lines 1-5; 43-55); and a memory module in communication with the CPU and the DMA module, the memory module including a first image capture buffer that temporarily stores first-in-time captured image data prior to displaying first-in-time image data and a second image capture buffer that temporarily stores second-in-time captured image data prior to displaying

second-in-time image data (Column 2, lines 5-25; Figure 1, element 300; Column 3, lines 19-22 (*image buffer*), 30-32 (*frame buffer for storing pixels of a displayed image*); 35-40; line 55 through Column 4, line 5; Column 5, lines 5-64, *double buffers;* Column 4, lines 63 through Column 5, line 12). The motivation for combining an imager with direct memory access and double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

Roth does not disclose temporarily storing via first image capture buffer accessible to the CPU and second image capture buffer accessible to the CPU. Anderson teaches temporarily storing via first image capture buffer accessible to the CPU and second image capture buffer accessible to the CPU (Figure 4, *storing raw and compressed image data, input buffers, variables used by the CPU,* Column 7, lines 35-60). The motivation for combining an imager with double buffers is to improve display speed and prevent tearing of the image in the display

(Column 7, lines 56-60). Anderson is evidence that at the time of the invention, it would have been obvious to one skilled in designing image storing and displaying machines, to combine the benefits of image storing and displaying, as Roth discloses, with double buffering, as Anderson teaches to improve displaying speed of multiple images and prevent tearing of these images as they are rapidly displayed.

6. Regarding claim 2, Roth discloses an image device of Claim 1, further comprising a display that displays to a user (see above). Roth does not disclose that the display is first-in-time image data followed by the display of second-in-time image data. Shand teaches that the display is first-in-time image data followed by the display of second-in-time image data (Column 5, lines 5-12, *can be recombined...at a later time for off-line processing of full 12 bit high precision images*).

The motivation for combining an imager with direct memory access and double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to

combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

7. Regarding claim 3, Roth discloses an image device of Claim 1, further comprising a field programmable array (FPGA) device that implements memory access (Column 13, lines 59-67). Roth does not disclose FPGA that implements the direct memory access (DMA) module. Shand teaches the FPGA that implements the direct memory access (DMA) module (Column 3, line 55 through Column 4, line 5).

The motivation for combining an imager with direct memory access and double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

8. Regarding claim 4, representative of claims 11, 17, 22, Roth discloses an image device of Claim 1, further comprising a means for enhancing image data stored in the first and second image capture buffers (Figures 10-14, *video RAM, static RAM, data buffers and latches,* Column 13, lines 40-67; Column 16, lines 43-51; Column 19, lines 45-50).

9. Regarding claim 5, representative of claims 12, 13, 19-21, 24, 25 and 27, Roth discloses an image device of Claim 1, further comprising a means for formatting image data stored in the first image capture buffer (*Sony CCIR format camera,* Column 8, lines 13-15). Roth does not disclose reformatting image data stored in the first and second image capture buffers. Shand teaches reformatting image data stored in the first and second image capture buffers (Abstract; Column 2, lines 5-25).

The motivation for combining an imager using FPGA with direct memory access and reformatting image data in double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42) and for handling various hardware formats in standard IEEE format (Column 6, lines 45-54). Shand is evidence that at the time of the invention, it

would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

10. Regarding claim 6, representative of claims 18, 23, 26, Roth discloses an image device of Claim 4, wherein the memory module further includes an image display buffer that temporarily stores captured image data that has been enhanced prior to display (see above). Roth does not disclose the memory module of claim 1. Shand teaches the memory module of claim 1 (see claim 1 above).

The motivation for combining an image enhancer using FPGA with direct memory access and reformatting image data in double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42) and for handling various hardware formats in standard IEEE format (Column 6, lines 45-54). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer

memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

11. Regarding claim 7, (see claim 1 above), Roth discloses a method for simultaneous image capture and image display in an imaging device (see above), the method comprising the steps of: capturing the first-in-time image data to a first image capture buffer that is in communication with an imager; capturing the second-in-time image data to a second image capture buffer that is in communication with an imager; and displaying the first-in-time image data on a display while the image device captures the second-in-time image data to the second image capture buffer ([image data may not be images but data about the imaging process], *video RAM* and *label image data*, Column 13, lines 40-67, Column 16, lines 33-37, 52-54; *static RAM (SRAM),* Column 14, lines 16- 47, *gain values*, Column 4, lines 12-14, 37-55, *the second memory includes a bin...to each possible intensity level*; Column 16, lines 28-35; Figure 11, Column 17, lines 35-37; Column 19, lines 46 through Column 20, line 6, , three distinct fields or exposures; data buffers, Column 20, lines 12-24).

12. Regarding claim 8, Roth discloses the method of Claim 7, further comprising the steps of: capturing third-in-time image data to the first buffer once the first-in-time image data is displayed and while the image device captures the third-in-time image data to the first buffer. (Column 15, lines 54-63). Roth does not disclose displaying the second-in-time image data on a display. Shand teaches displaying the second-in-time image data on a display (see above, Column 4, lines 38-42).

The motivation for combining an image enhancer using FPGA and three sequential image frames with direct memory access and reformatting image data in double buffers is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42) and for handling various hardware formats in standard IEEE format (Column 6, lines 45-54). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

13. Regarding claim 9, representative of claims 10, 14-16 (see claim 1 above), Roth discloses a method of Claim 7, wherein capturing first-in-time image data to a first image capture buffer (see above) and an end-of-frame signal (*VDRV* and *HDRV signals*, Column 8, lines 44-46).

Roth does not disclose further comprises the step of: issuing, at a CPU, a capture command to a DMA module to capture first-in-time image data to the first image capture buffer; queuing, at the DMA module, the capture command until the DMA module receives an end-of-

frame signal; executing, at the DMA module, the capture command to capture first-in-time image data to the first image capture buffer; and transferring the first-in-time image data from the imager to the first image capture buffer. Shand teaches further comprises the step of: issuing, at a CPU, a capture command to a DMA module to capture first-in-time image data to the first image capture buffer (Column 3, lines 5-32); queuing, at the DMA module, the capture command until the DMA module receives an end-of-frame signal (*size of transfer, buffer full*, Column 3, line 55 through Column 4, line 56); executing, at the DMA module, the capture command to capture first-in-time image data to the first image capture buffer; and transferring the first-in-time image data from the imager to the first image capture buffer (*transfer complete*; Column 5, lines 30-32, 51-64); furthermore (Claim 16), issuing a fourth command to capture fourth-in-time image data to the second image capture buffer (there are only two); executing the third capture command [which is a repeat of the first], (*address of memory pages of the image buffer, the list of command blocks is not contiguous, the next field can store the address of the next command block in a linked list. The command blocks can be considered an instruction stream for operating the DMA controller.* [The device taught by Shand operates in real time on a cycle or continuous sequence, meaning a fourth command would follow the third which will follow the second which will follow the first] (Column 4, lines 43-56; Column 6, lines 27-54).

The motivation for combining an image enhancer using FPGA, three sequential image frames and end-of-frame signals with direct memory access, reformatting image data in double buffers and capture commands is (1) to enable reading high precision images as fast as possible (Column 1, lines 30-37); (2) to enable real-time software format processing of image data (Column 1, lines 38-48); (3) to transport the combinations of the first portions of the input digital

signals as output digital signals to the memory of the computer system (Column 2, lines 22-25). DMA enables data signals to be transported from a source to a destination with minimal utilization of processor resources (Column 4, lines 3-5). The double buffers enable receiving pixel data from a converter, while the other buffer is transporting packets to the image buffer of the memory (Column 4, lines 38-42) and for handling various hardware formats in standard IEEE format (Column 6, lines 45-54). Shand is evidence that at the time of the invention, it would have been obvious to one skilled in the art of precision image acquisition processing and display to combine the benefits of image acquisition hardware with double buffer memory scheme to achieve faster and more precise processing and image display of multiple data formats (*pixel widths,* Column 3, lines 50-55; Column 6, lines 15-54).

***Response to Arguments***

14. The Applicant is respectful in asserting that in the amended claims, time-sequential capturing and storing of multiple images using double buffers accessible to the CPU for quickly drawing the images is not explicitly revealed by the first office action references Roth and Shand (Page 10, 3rd – 4th Paragraphs, Page 11, 1st Paragraph; Pages 12-20).

The Examiner respectfully notes the newly amended claim language and offers another reference, Anderson, that, in combination with Roth and Shand, does explicitly teach capturing and storing multiple images using double buffers accessible to the CPU to speed up the displaying of multiple images without tearing (Anderson, Column 7, lines 35-60) in a digital camera system (Abstract).

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**Or FAX'd to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

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February 27, 2004

MATTHEW C. BELLA
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